

Review of Fin FET Technology and Circuit Design Challenges

¹Bibin Lawrence R, ²Jency Rubia J

1,2M.E-VLSI Design Vel Tech Multi Tech Dr.Rangarajan Dr.Sakunthala Engineering College, Avadi, Chennai-600 062, India

ABSTRACT

Considering the difficulties in planar CMOS transistor scaling to secure an acceptable gate to channel control FinFET based multi-gate (MuGFET) devices have been proposed as a technology option for replacing the existing technology. The desirability of FinFET that its operation principle is same as CMOS process. This permits to lengthening the gate scaling beyond the planar transistor limits, sustaining a steep subthreshold slope, better performance with bias voltage scaling and good matching due to low doping concentration in the channel. There are, still, several challenges and limitations that FinFET technology has to face to be competitive with other technology options: Fin shape, pitch, isolation, doping, crystallographic orientation and stressing as well as device parasitic, performance and patterning approaches will be discussed.

Keywords – FinFET, Fin patterning, Fin shape, SRAM design, Circuit challenges

I. INTRODUCTION

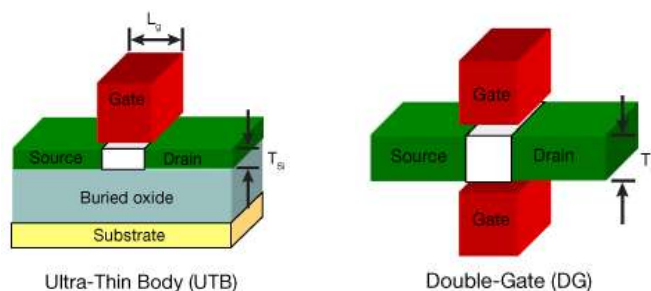
Today mobile and computing markets continue to innovate at a dramatic rate delivering more performance in smaller form factors with higher power efficiencies. According to Moore's law, the number of transistors in an area should double every months. To make this into reality, transistors should get shrink in size to accommodate double the number per unit area. While scaling down the device channel length, the short channel effects are raised [1]. As the technology scaling continues, FinFET is known to be a probable alternative to solve the problems related to short channel effects of planar technology [2]. FinFET is a developing new technology and the memory circuits started to occupy a major area of chip. So, it is very important to have an overall literature review to understand the progress of FinFET technology, circuit and manufacturing challenges.

This paper is organized as follows. Section II describes the FinFET technology and the brief history of FinFET. Section III clarifies the manufacturing challenges and section IV explains about the circuit design challenges. Finally section V shows the summary of this review paper.

II. LITERATURE REVIEW

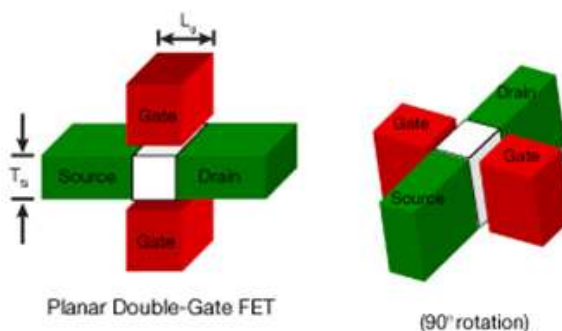
2.1 FinFET Technology:

In 1990s UC Berkeley team led by Dr. Chamming Hu proposed a new structure for the transistor that would reduce leakage current. This team thought that a thin body MOSFET structure would control short channel effects and suppress leakage by keeping the gate capacitance closer to the whole channel. Keeping that, they proposed two possible structures shown in fig 1.



By rotating the DG structure, we can achieve the lowest gate leakage current. As the gate electrodes become self-aligned, it supports easier manufacturing using standard lithography techniques in fig 2.

Modern FinFETs are 3D structures that rise above the planar substrate. Providing the good control of the conducting channel by the gate, which wraps around the channel, very little current is allowed to leak through the body when the device is in the off state. Other research teams have shown that the scaling of FinFETs gate length is relative to the thickness of the channel. For instance, KAIST has demonstrated a 3nm FinFET in its lab.



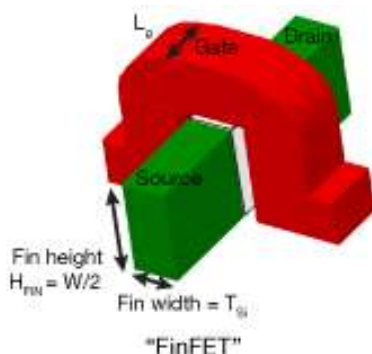


Fig 2: scaling of FinFET

2.2 History of FinFETs

The research of multi-gate MOSFET happened about quarter century ago, in late 1980's. The first multi-gate transistor was that published by Hieda et al [3] in 1987. From that paper authors realized that fully depleted body of silicon based transistor helps to improve switching due to lessened body bias effect. Two years later, Hisamoto et al [4] demonstrated an ancestor of FinFET- first double gate transistor, in bulk silicon, called DELTA. First FinFET on SOI substrate was published a decade later [5]. SOI also enables horizontal gate-all-around (GAA) transistor [6] creating a precursor to silicon nanowire devices. Stacking more than one nanowire on top of each other demonstrated increased drive current capability for a given foot-print size of a transistor [7]. The first protest of FinFET circuit was a 4-stage inverter by Rainey et al in 2002 [8] and the earliest report of FinFET ring oscillator was published by Nowak et al [9]. FinFET SRAM cells have been reported in 2002 [10] and 20 MB SRAM array in 2004 [11].

III. MANUFACTURING CHALLENGES

Almost every aspect of device technology is affected by transitioning from planar to fin device architecture. Here, some of the key issues.

3.1 Fin patterning

In order to match or exceed effective width of a FinFET device, their fins needed to be very tall. Generally, formation of two fins per minimum pitch allows reasonable fin aspect ratio that meets or exceeds effective width of corresponding planar device. Lithographic patterning of such fins has several drawbacks:

Double patterning is required to halve the minimum pitch but it brings overlay error between two fin patterns. This error could lead to unwanted fin pitch variation that impacts down- stream processing. If the selected fin width (twice smaller than gate length) is below well controllable capabilities of optical lithography, resulting in poor fin width control. Line edge roughness (LER) of the

process leads to considerable local fin width variability (LWR).

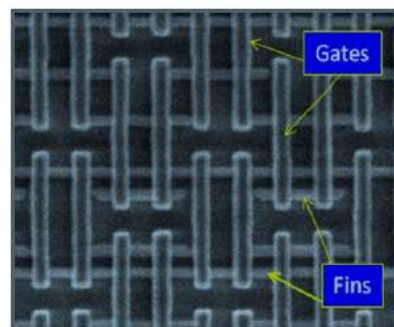


Fig 3: Fin Width Variability

3.2 Fin shape

The first FinFET based high performance logic product - Intel's 22nm node microprocessor has been built with FinFET sidewalls sloping at about 8 degrees from vertical. Such shape has several practical reasons for manufacturability of this technology:

Fins with lower aspect ratio (height: width) are more robust mechanically thus less exposed to damage processing. Sloping sidewalls assure better fill of trenches between fins with fin isolation dielectric.

Etching gate spacer off fin sidewalls (if desired) is easier than for vertical fins. Gate etch, which in FinFETs requires much more easier. Sloping fin sidewall has a significant drawback – poor short channel control toward the bottom of the fin [12] fig Such fins would usually require additional doping to lessen this problem. Thus causing increased random dopant fluctuation. The drawback of sloping fin sidewalls will become more serious with scaling gate length and will need to migrate toward more vertical shape.

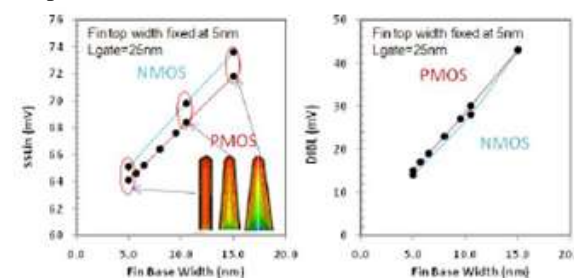


Fig 4: Significant Drawback

2.3 Fin dimension variability

Device's effective electrical width is directly related to fin height. Of the two, fin height variation generally more critical [13]. Hence, any fin height variation directly transfer to device width variation. Unlike in planar devices, where active area patterning variation affects only the narrowest of transistors, all

fin-based devices suffer from the same percentage of device width error.

3.4 Device doping

Preferably, one would desire no doping in FinFET channel. However, some light doping is required to set alternative threshold voltages for better control of leakage current. Those doping are done by implantation. Source/drain doping requires high doses of dopant, thus increase series resistance. This caused implant damage in the fins that, due to fin's geometry. High temperature (300-400C) implants called plasma-based doping or monolayer doping methods deliver dopants with less damage to the fin. Alternatively, in-situ doped epitaxial material is deposited in source/drain area to deliver the dopant. This can be done with or without removal of the fin in source/drain area prior to epitaxial material.

3.5 Stress for fins

Stressing fins is generally less effective than in planar devices and further diminishes with gate pitch and fin size scaling. Application of stress from under the fin channel by lattice-mismatched epitaxial buffer material is more effective than source/drain stressors in scaled FinFETs [14]. Single SRB solution for NMOS and PMOS FinFET is forecasted possible with SiGe SRB where Ge concentration is in mid-range of about 40-50%. It provides tensile strain to Si fin for NMOS grown on top of it and compressive stress for SiGe with high concentration of Ge or a pure Ge fin grown for PMOS [15].

3.6 Orientation of fins

Nominal orientation of fins, along $\langle 110 \rangle$ direction on (100) wafers results in finfet current flowing on (110) sidewall surfaces. Hole mobility is sizably higher on (110) surface on (100) but difference decreases with increasing strain [16]. Electrons flow somewhat slower along (110) plane than on (100) in planar devices. However, in FinFETs, quantum confinement results in quite different behavior – electron mobility becomes comparable or better for (110) sidewall conduction than for (100) [17]. Growth of epitaxial material on (100) fin surfaces results in uniform thickness increase that might be desired in some situation than that of diamond-shaped structures grown on (110) walls.

3.7 FinFET parasitic capacitance

FinFET has inherently higher parasitic capacitance than planar device. It consists of gate-to-fin capacitance between part of the gate above the fin and the top of the fin. This capacitance decreases with decreasing fin pitch and increasing fin height, per effective device width [18,19]. Bulk finfet junction capacitance between source/drain area and

device well/substrate could be several times smaller than in planar devices.

3.8 Reliability

FinFET fully depleted operation provides lower transverse field in the device. This leads to improve NMOS reliability for dielectric breakdown (TDDB) as well for threshold voltage instability (PBTI) observed in transition from planar 32nm to FinFET based 22 nm technology node. PMOS reliability for both TDDB and NBTI appears unchanged for FinFETs [20].

IV. CIRCUIT DESIGN CHALLENGES

Converting planar device layouts to fins, faces the challenge of describing transistor widths in digital fashion. Generally, wide devices consist of large number of fins, so the effective width has to face redesign challenge. Narrow devices and particularly SRAM transistors will face major redesign. All FinFETs on the wafer will have the same height for ease of processing; however, the 3D FinFET offers another dimension in designing FinFET devices. Taller fins can deliver more effective device width than planar ones. This design knob can either deliver better layout density than planar device or increase amount of drive current per given foot print. As we mentioned, since we are using taller fins, parasitic capacitance reduced.

4.1 SRAM

The SRAM cells started to face challenges when device scaling started to take place. Again, planar technology eventually failed to meet the requirements with device scaling. The FinFET technology is one of the emerging techniques in this situation. There are many device approaches of FinFETs namely Tunnel FinFET (TFET), junction less FinFET, pseudo-spin FinFET. By using these device approaches in the SRAM cells, we can overcome the SCE in the SRAM. Supply voltage scaling is possible for TFET without increasing the static power consumption [21]. For SRAM circuit, it is recommended to use 8T/10T cell to achieve the desired read/write noise margin instead of 6T cell for TFETs. In [22], the authors demonstrated a FinFET based pseudo-spin transistor or pseudo-spin FinFETs (PS-FinFETs) and he investigated that is a non-volatile SRAM cell. Junction less FinFETs (JL FinFETs) experience less process complexity than inversion mode FinFETs (IM FinFETs). In [23], they reported that JL-FinFET exhibits better short channel characteristics and higher ON-OFF current ratio compared to IM FinFETs.

4.2 FinFET Design Ecosystem

Most of Electronic Design Automation (EDA) tools needs to be adapted for FinFET designs. This

process has been largely completed and tools are available from key vendors (Synopsis, Mentor Graphic and Cadence). Leading semiconductor foundries are capable of providing full EDA support for their customers.

V. Summary

FinFET technology has entered the market. High performance logic has adapted this device and will continue to use it for several generations into the future. New materials for fins are likely to be introduced into products in this decade. Substantial changes are brought up into circuit design world by FinFET and design ecosystem is rapidly maturing with tools updates.

REFERENCES

- [1] Y.Taur and T.H.Ning, "Fundamentals of modern VLSI Devices" New York: Cambridge Univ. Press, 1998.
- [2] "Design of High-performance digital logic circuits based on FinFET technology", International Journal of Computer Applications, pp 40-44 March 2012.
- [3] K. Hieda et al., IEDM Tech. Dig., p. 736 (1987)
- [4] D. Hisamoto et al. IEDM Tech. Dig., p. 833 (1989)
- [5] D. Hisamoto et al. IEDM Tech. Dig., p. 1032 (1998)
- [6] J.-P. Colinge et al., IEDM Tech. Dig. p. 595 (1990)
- [7] S.-Y. Lee et al., VLSI Technol. Dig., p. 200 (2004)
- [8] B. Rainey et al., Dev. Res. Conf. Proc., (2002)
- [9] E. Nowak et al., IEEE CiCC Conf. Proc., p. 339 (2003)
- [10] E. Nowak et al., IEDM Tech. Dig., p. 411 (2002)
- [11] J.A. Choi, et al., IEDM Tech. Dig., p. 647 (2004)
- [12] Y. Li and W-H. Chen, NSTI-Nanotech 2006, Vol. 3, (2006)
- [13] C-Y.Kang et al., Symp. VLSI Technol. Dig., p. T90 (2013)
- [14] G. Eneman et al., IEDM Tech. Dig., p.131 (2012)
- [15] G. Eneman et al., Symp. VLSI Technol. Dig., p.92 (2013)
- [16] P. Packan et al., IEDM Tech. Dig., p.63 (2008)
- [17] C.D. Young et al., Symp. VLSI Tech. Dig., p. 18 (2011)
- [18] M. Guillorn et al., Symp. VLSI Technol. Dig. p. 12 (2008)
- [19] C-Y. Kang et al., Symp. VLSI Technol. Dig., p.90 (2013)
- [20] S. Ramey, et al., IRPS (2013)
- [21] Shuto, Y. et al, "FinFET-based pseudo-spin-transistor: Design and performance" (ISCDG), 2013.
- [22] Kerber, P. et al, "Strained SOI FinFET SRAM Design" Electron Device Letters, IEEE (Volume:34 , Issue: 7), pp: 876– 878, 2013.
- [23] Ming-Hung Han et al, "Device and Circuit Performance Estimation of Junctionless Bulk FinFETs", Electron Devices, IEEE Transactions on (Volume:60 , Issue:6), pp: 1807 – 1813, 2013.